

Dhruv Baronia

Portfolio: <https://dhruvbaronia.com>

Github: github.com/boronhub

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EDUCATION

- **University of Illinois at Urbana-Champaign** Urbana, Illinois
Masters of Science - Computer Science August 2024 - May 2026
Advisor: Prof. Vikram Adve
- **University of Illinois at Urbana-Champaign** Urbana, Illinois
Bachelor of Science - Computer Science and Linguistics August 2021 - May 2024
Courses: Parallel Programming (CS 483), ML for Compilers and Architecture (CS 598), Computer Systems Engineering (ECE 391), Algorithms & Models of Computation (CS 374), Programming Language Design (CS 422), Advanced Compiler Construction (CS 526),
Extracurriculars: SIGPwny (Cybersecurity club); Intro to C++ - Course Assistant, Crossword Club - Treasurer, PizzaFM(College Radio) - DJ and Staff Writer, The Daily Illini (School newspaper) - Staff Writer
GPA: 3.6/4.0

SKILLS SUMMARY

- **Languages:** C/C++, Rust, Python, Racket, Haskell, Java, OCaml, Bash, Dart
- **Frameworks:** LLVM, MLIR, XLA, ONNX, TensorFlow, PyTorch, CUDA, egg, Rosette, Z3, K Framework
- **Tools:** Linux, CMake, PyTest, Catch2, AWS, GCP, Grafana, Prometheus, Docker, git, PostgreSQL, MongoDB, ZMQ

PUBLICATIONS

Kothari, Akash, Abdul Rafae Noor, Muchen Xu, Hassam Uddin, Dhruv Baronia, Stefanos Baziotis, Vikram Adve, Charith Mendis, and Sudipta Sengupta (2024). "Hydride: A Retargetable and Extensible Synthesis-based Compiler for Modern Hardware Architectures". In: *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*. ASPLOS '24. New York, NY, USA: Association for Computing Machinery, pp. 514–529. ISBN: 9798400703850. DOI: 10.1145/3620665.3640385. URL: <https://doi.org/10.1145/3620665.3640385>.

EXPERIENCE

- **Cadence Design Systems** Austin, TX
Compiler Engineering Intern May- Aug 2023, 2024
 - **ML Compiler Backend:** Added support for generic CPUs + NeoNPU accelerator platform in Xtensa Neural Network Compiler; created new linker scripts and backends
 - **MLIR:** Conversion passes for lowering 20+ ML operations to optimized library calls
 - **Constant Handling:** Implemented handling for raw constant data parsed from ONNX files and loading it into a JIT pipeline for optimization
 - **GLOW:** Modified GLOW internals to generate end-to-end tests using custom ops
- **Advanced Micro Devices, Inc. (AMD)** San Jose, CA
Compiler Engineering Intern May 2022 - Aug 2022
 - **MLIR:** Writing MLIR passes for various internal dialects and developing a new graph-based dialect. Created a new dialect for lowering logical graph representation to hardware level
 - **Memory Allocation:** Worked on scheme for memory allocation and routing on AIE devices
 - **ML Compilers:** Gained experience on the flow for ML compilers, from understanding various ops at the IR level to how we can optimize them at the hardware level
- **LLVM Research Group at UIUC** Urbana, IL
Research Assistant Feb 2022 - Present
 - **ASPLOS'24 Paper:** : Hydride: A Retargetable and Extensible Synthesis-based Compiler for Modern Hardware Architectures
 - * Ported HPC benchmarks to Halide
 - * Integrated external libraries for x86 fuzzer tests
 - * Worked on code synthesis using a Racket DSL
 - * Set up build system for project using Makefiles and Python scripts
 - **Current Research:** : Developing optimized compilers for neural network accelerators using program synthesis and equality saturation
 - **Tensor Extensions to LLVM:** Working on XLA frontend for retargetable tensor code generation framework for LLVM (TLX)
 - **Heterogenous Compilers:** Wrote 10+ tests and passes for the release for Heterogeneous Parallel Virtual Machine (HPVM) tool